REMARKS

On July 26, 2004, the Patent Office mailed applicants a Restriction Requirement. On August 11, 2004, applicants mailed a Response to the Restriction Requirement. According to the Patent Office's online "PAIR" system, applicants' Response was received at the Patent Office on August 16, 2004. According to PAIR, the Patent Office mailed a non-final Office Action to applicants on November 18, 2004. Applicants received the November 18, 2004 Office Action on November 22, 2004.

The first page of the November 18, 2004 Office Action bears a "date mailed" date of July 26, 2004. The "date mailed" date of July 26, 2004 is erroneous and is apparently a holdover from the Restriction Requirement mailing date. Applicants received the November 18, 2004 Office Action on November 22, 2004. Moreover, status item 1 of the Office Action Summary page of the November 18, 2004 Office Action indicates that the November 18, 2004 Office Action is responsive to the communication filed on August 16, 2004. The November 18, 2004 Office Action also includes an initialed copy of applicants' Information Disclosure Statement Form PTO-1449, which bears a "date considered" date of November 12, 2004. As these dates demonstrate, the July 26, 2004 "date mailed" date listed on the

first page of the November 18, 2004 Office Action is a clerical error. Applicants are therefore treating the November 18, 2004 Office Action as being mailed November 18, 2004, as established by the PAIR records.

The present application was filed with 23 claims. Following the Restriction Requirement, claims 19-23 were withdrawn from consideration.

In the November 18, 2004 Office Action, claims 10-18 were allowed. Claims 5, 7, and 8 were objected to as being dependent upon a rejected base claim, but were indicated to be allowable if rewritten in independent form including the limitations of the base claims and any intervening claims. Claims 1-4, 6, and 9 where rejected under 35 U.S.C.§102(e) as being anticipated by Novosel et al. US 2004/0100849 A1 ("Novosel").

Applicants reserve the right to pursue the subject matter of claims 5, 7, 8 (e.g., by placing claims 5, 7, and 8 in independent form) should the present Reply not be considered to place the application in condition for allowance. The rejections of claims 1-4, 6, and 9 under 35 U.S.C. §102(e) are respectfully traversed.

Applicants' invention relates to programmable antifuses. Such devices may be use to permanently switch redundant circuitry into place to fix a reparable defect during

integrated circuit manufacturing operations. Programmable antifuses may also be used to program a serial number or other information into an integrated circuit.

With conventional arrangements, lasers are sometimes used to program antifuses. The equipment used to program antifuses with lasers can be complex and expensive, so attempts have also been made to form electrically-programmable antifuses. With one conventional approach, antifuses are formed using metal-oxide-semiconductor (MOS) transistor structures having thin gate dielectrics that are ruptured by application of a large electric field. Rupturing the gate dielectric creates an electrical short that programs the antifuse.

There are problems associated with dielectric breakdown programming. For example, as applicants describe in their specification at page 11, lines 2-10, in conventional dielectric breakdown antifuse arrangements, there is a risk of damage to the integrated circuit's dielectric stack when the antifuse is programmed. Dielectric breakdown arrangements also require fairly large programming voltages. The fabrication of dielectric-breakdown antifuses may also require the use of undesirable process steps.

Applicants' invention addresses these concerns by using a different antifuse arrangement. In particular, as applicants explain at lines 9-29 on page 5 of their

specification, applicants' approach involves biasing an antifuse transistor to create a sufficient current flow to induce localized substrate melting. Substrate melting programs the antifuse, rather than dielectric breakdown. The localized melting is induced by biasing the antifuse's substrate terminal to inject carriers into the substrate under the antifuse transistor's gate. The injected carriers turn the transistor on and produce a high current between the drain and source of the antifuse transistor.

Claim 1 is directed to this aspect of applicants' invention.

In particular, claim 1 is directed to electrically-programmable integrated circuit antifuse circuitry formed from a semiconductor that includes a metal-oxide-semiconductor antifuse transistor having a drain, source, gate, and substrate. In the antifuse transistor of claim 1, the drain and substrate form a drain-substrate p-n junction. As specified by claim 1, there is circuitry connected to the antifuse transistor that applies a voltage to the drain that causes avalanche breakdown of the drain-substrate p-n junction and a rise in voltage at the substrate that turns the antifuse transistor on and produces sufficient current between the drain and source to melt the semiconductor and program the antifuse.

The circuitry and methods of Novosel do not show or suggest the features of claim 1. Novosel uses a conventional dielectric-breakdown antifuse transistor arrangement. FIG. 2 of Novosel shows a non-volatile memory element 200 based an antifuse element transistor M1. Novosel's transistor has a drain (node 6), source (node 5), and gate (node 4). To program Novosel's transistor, a voltage is applied between the source and the gate. As described at page 3, paragraph 23 of Novosel, if a sufficiently high field is applied, the dielectric (oxide) will break down, so that it conducts current.

Novosel describes several variations of a dielectric-breakdown antifuse structure.

With one of Novosel's arrangements, the source and drain are both grounded, so the field impressed across the gate dielectric is uniform. This type of arrangement is shown in FIG. 3A. In this case, no current can flow between source and drain, because the source and drain are at the same voltage.

Another of Novosel's arrangements uses slightly different source and drain voltages during programming. This type of arrangement is shown in FIG. 3B. As shown in FIG. 3B, when a voltage of 2V is applied to the drain terminal while the source is grounded, a voltage gradient develops under the gate. As a result, the voltage across the gate dielectric of the antifuse transistor structure of FIG. 3B becomes concentrated

near the source. According to Novosel, this crowds the programming current through the gate dielectric into the area near the source. (See, for example, page 4, paragraph 34 of Novosel.) The programming current in the arrangement of FIG. 3B flows through the dielectric and does not flow between drain and source to melt the substrate under the gate.

Additional variations of Novosel's antifuse structures are shown in FIGS. 4A and 4B. Both of these variations attempt to create a more focused electric field through the gate dielectric to enhance programming. The arrangement of FIG. 4A uses two gates 403 and 405 to create a more focused electric field under part of the gate. The arrangement of FIG. 4B attempts to form a voltage gradient in the source 306.

As these FIGS. and the associated description in Novosel make clear, Novosel's approach does not program by melting. Rather, Novosel uses the conventional dielectric breakdown mechanism to rupture a gate dielectric. Claim 1 specifies that applicants' programming operations are performed by generating a current sufficient for melting that flows between drain and source, while Novosel's programming current flows between Novosel's source and gate through Novosel's gate dielectric. Claim 1 specifies how the melting current is produced between source and drain. In particular, claim 1 makes it clear that a voltage is applied to the drain that causes

avalanche breakdown of the drain-substrate p-n junction and a rise in voltage at the substrate that turns the antifuse transistor on. Novosel does not show or suggest that avalanche breakdown occurs in Novosel's device, let alone avalanche breakdown of Novosel's drain substrate p-n junction. For each of these reasons, claim 1 is not anticipated by Novosel and is allowable. Rejected claims 2-4, 6, and 9 and claims 5, 7, and 8 depend from claim 1 and are therefore also allowable.

The foregoing demonstrates that claims 1-18 are in condition for allowance. This application is therefore in condition for allowance. Reconsideration of this patent application and allowance are respectfully requested.

Respectfully submitted,

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